CLAIMS

1. A method of fabricating an SOI structure which comprises the steps of:

(a) providing a substrate and a device wafer;

(b) forming an electrically insulating layer having an outer face on one of said substrate or said device wafer, said electrically insulating layer having an electrical interconnect structure therewithin, a portion of said interconnect structure extending substantially to said outer face of said electrically insulating structure; and

(c) bonding said outer surface of said electrically insulating layer to the other of said substrate or device wafer.

2. The method of claim 2 wherein a portion of said electrically insulating layer is disposed between said interconnect structure and at least one of said substrate or device wafer, further including the step of applying a voltage across said portion of said electrically insulating layer sufficient to break down said portion of said electrically insulating layer while maintaining the integrity of the remainder of said SOI structure

3. The method of claim 1 wherein at least one of said device layer and said substrate includes a bond region, said interconnect structure contacting said bond region.

4. The method of claim 2 wherein at least one of said device layer and said substrate includes a bond region, said interconnect structure contacting said bond region through said portion of said electrically insulating layer..

5. An SOI structure comprising:

(a) a device layer having a surface;

(b) a substrate;

(c) an electrically insulating layer separating said device layer from said substrate and immediately adjacent said surface of said device layer; and

(d) an electrical interconnect within said electrically insulating layer electrically connecting said substrate to said surface of said device layer.

6. The structure of claim 5 wherein a portion of said interconnect is through a broken down dielectric.

7. A method of forming an SOI structure having a device layer, a substrate and an electrically insulating layer separating a portion of said device layer from said substrate, comprising the steps of:

(a) forming a substantially planar surface comprising areas of one of said device layer and said substrate and areas of said electrically insulating layer; and

(b) bonding said surface to the other of said substrate wafer and device layer.

8. The method of claim 8 further including the step of forming an electrical interconnect structure in said electrically insulating layer, said interconnect structure contacting at least one of said device layer and said substrate.

9. The method of claim 7 further including the step of forming an electrical interconnect structure in said electrically insulating layer, said interconnect structure contacting both said device layer and said substrate.

10. A method of forming an electrically conducting via, comprising the steps of:

(a) providing a layer of electrically insulating material having a surface;

(b) forming an edge extending from said surface through said layer of electrically insulating material;

(c) forming a layer of electrically conductive material on said edge;

(d) performing a patterned etch to selectively remove electrically conductive material, leaving said material where the conducting via is desired;

(e) depositing additional electrically insulating material; and

(f) planarizing said surface.

11. The method of forming the electrically conducting via of claim 10, further including the steps of providing a device layer and a handle wafer, and separating said device layer from said handle wafer with said electrically insulating material.

12. An integrated circuit which comprises:

(a) a device layer;

(b) a substrate spaced from said device layer;

(c) a buried dielectric having an interconnect, said dielectric bonded to one of said device layer and said substrate to form an interface with said one of said device layer and said substrate; and

(d) an electrically conductive path across said interface and disposed directly beneath said device layer.

13. The circuit of claim 12 wherein said electrically conductive path contacts the other of said device layer and said substrate.

14. The circuit of claim 12 wherein said electrically conductive path is an extension of said device layer.

15. The circuit of claim 13 wherein said electrically conductive path is an extension of said device layer.

16. The circuit of claim 12 wherein said substrate is a semiconductor substrate.

17. The circuit of claim 12 wherein said substrate comprises a semiconductor substrate and a dielectric.

18. A method of fabricating an integrated circuit which comprises the steps of:

(a) providing a device layer;

(b) providing a substrate spaced from said device layer;

(c) bonding a buried dielectric having an interconnect therein to one of said device layer and said substrate to form an interface with said one of said device layer and said substrate; and

(d) forming an electrically conductive path across said interface to said interconnect directly beneath said device layer.

19. The method of claim 18 wherein said electrically conductive path contacts the other of said device layer and said substrate.

20. The method of claim 18 wherein said electrically conductive path is an extension of said device layer.

21. The method of claim 19 wherein said electrically conductive path is an extension of said device layer.

22. The method of claim 18 wherein said step of forming an electrically conductive path across said interface to said interconnect is formed by breakdown of said dielectric.

23. The method of claim 18 wherein said substrate is a semiconductor substrate.

24. The method of claim 18 wherein said substrate comprises a semiconductor substrate and a dielectric.